Amendment 3/24/95
to Permit 3495

Exhibit B

EXHIBIT 3

OFGS File No.: IR 2.064 (2-838)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of:

ALEXANDER LIDOW et al.

Patent No.: 5,008,725

Reexamination Control No.: 90/003,495

Filing Date: July 15, 1994

Examiner: CARROLL, J.

Group Art Unit: 2508

AMENDMENT PURSUANT TO
37 C.F.R. § 1.550(b)

Enclosure: Postcard

Box Reexam
Hon. Commissioner of
Patents and Trademarks
Washington, DC 20231

Sir:

Responsive to the Office Action mailed January 25, 1995, please amend claims 1, 3, 7 and 8 of U.S. Patent No. 5,008,725 as follows:

1. (Amended) A high power MOSFET device having more than 1000 parallel-connected individual FET devices closely packed into a relatively small area comprising:

a thin wafer of semiconductor material having first and second spaced, parallel planar surfaces; at least a first portion of the thickness of said wafer which extends from said first planar surface consisting of an epitaxially deposited region of a first conductivity type;

a plurality of equally spaced symmetrically disposed laterally distributed *identical* hexagonal base regions each having a second conductivity type formed in said epitaxially deposited region and extending for a given depth beneath said first planar surface, the space between said polygonal base regions defining a vertical common conduction region of said first conductivity type extending downwardly from said first planar surface;

said hexagonal base regions spaced at said first surface from surrounding ones by a symmetric hexagonal lattice of semiconductor material of said first conductivity type;

said lattice being continuous and uninterrupted;

each side of each of said hexagonal base regions being parallel to an adjacent side of another of said hexagonal base regions;

a hexagonal annular source region of said first conductivity type formed in an outer peripheral region of each of said hexagonal base regions and extending downwardly from said first planar surface to a depth less than the depth of said base regions;

an outer rim of each of said annular source regions being radially inwardly spaced from an outer periphery of its respective hexagonal base region to form an annular channel between each of said outer rims of said annular source regions and said symmetric hexagonal lattice of semiconductor material of said first portion of said wafer;

a common source electrode formed on said first planar surface and connected to a plurality of said annular source regions and to interiorly adjacent surface areas of their said respective hexagonal base regions;

a drain electrode connected to said second planar surface of said wafer;

an insulation layer means on said first planar surface and overlying at least said annular channels; and

a polysilicon gate electrode atop said insulation layer means and operable to invert said annular channels.

3. (Amended) A high power MOSFET device having more than 1000 parallel-connected individual FET devices closely packed into a relatively small area comprising:

a thin wafer of semiconductor material having first and second spaced, parallel planar surfaces; at least a first portion of the thickness of said wafer which extends from said first planar surface consisting of an epitaxially deposited region of a first conductivity type;

a plurality of equally spaced symmetrically disposed laterally distributed *identical* polygonal base regions each having a second conductivity type formed in said slightly doped region and extending for a given depth beneath said first planar semiconductor surface, the space between said polygonal base regions defining a vertical common conduction region of said first conductivity type extending downwardly from said first planar surface;

said polygonal base regions spaced at said first surface from surrounding ones by a symmetric polygonal lattice of semiconductor material of said first conductivity type;

said lattice being continuous and uninterrupted;

each side of each of said polygonal base regions being parallel to an adjacent side of another of said polygonal base regions;

a polygonal annular source region of said first conductivity type formed in an outer peripheral region of each of said polygonal base regions and extending downwardly from said first planar surface to a depth less than the depth of said base regions;

an outer rim of each of said annular source regions being radially inwardly spaced from an outer periphery of its respective polygonal base region to form an

annular channel between each of said outer rims of said annular source regions and said symmetric polygonal lattice of semiconductor material of said first portion of said wafer;

a common source electrode formed on said first planar surface and connected to a plurality of said annular source regions and to interiorly adjacent surface areas of their said respective polygonal base regions;

a drain electrode connected to said second planar semiconductor surface of said wafer;

an insulation layer means on said first planar surface and overlying at least said annular channels; and

a polysilicon gate electrode atop said insulation layer means and operable to invert said annular channels.

7. (Amended) A vertical conduction high power MOSFET device exhibiting relatively low on-resistance and relatively high breakdown voltage; said device comprising:

a wafer of semiconductor material having planar first and second opposing semiconductor surfaces; said wafer of semiconductor material having a relatively lightly doped major body portion for receiving junctions and being doped with impurities of a first conductivity type;

a plurality of highly packed, equally spaced symmetrically disposed identical polygonal base regions of a second conductivity type formed in said wafer, each extending from said first planar semiconductor surface to a first depth beneath said first planar semiconductor surface; said polygonal base regions spaced from surrounding ones by a symmetric polygonal lattice of semiconductor material of said first conductivity type;

said lattice being continuous and uninterrupted; the space between adjacent ones of said polygonal base regions defining a vertical common conduction region of said first conductivity type extending downwardly from said first planar semiconductor surface;

a respective polygonal annular source region of said first conductivity type formed within each of said polygonal base regions and extending downwardly from said first planar semiconductor surface to a depth less than said first depth; each of said

polygonal annular source regions being laterally spaced along said first planar semiconductor surface from the facing respective edges of said common conduction region thereby to define respective coplanar annular channel regions along said first planar semiconductor surface between the polygonal sides of each of said polygonal annular source regions and said common conduction region;

a common source electrode means connected to said polygonal annular source regions and their respective base regions;

gate insulation layer means on said first planar semiconductor surface, disposed at least on said coplanar channel regions;

gate electrode means on said gate insulation layer means and overlying said coplanar channel regions;

a drain conductive region remote from said common conduction region and separated therefrom by said relatively lightly doped major body portion and extending to said second semiconductor surface; and

drain electrode coupled to said drain conductive region.

8. (Amended) A high power MOSFET device exhibiting relatively low on-resistance and relatively high breakdown voltage; said device comprising:

a wafer of semiconductor material having planar first and second opposing semiconductor surfaces; said wafer of semiconductor material having a relatively lightly doped major body portion for receiving junctions and being doped with impurities of a first conductivity type;

at least first and second spaced base regions of a second conductivity type formed in said wafer and extending downwardly from said first planar semiconductor surface to a first depth beneath said first planar semiconductor surface; the space between said at least first and second spaced base regions defining a vertical common conduction region of a first conductivity type at a given first planar semiconductor surface location; said common conduction region extending downwardly from said first planar semiconductor surface;

the surface of said common conduction region being continuous and uninterrupted and of said first conductivity type;

first and second annular source regions of said first conductivity type formed in said first and second spaced base regions respectively at said first planar semiconductor surface locations to a depth less than said first depth; said first and second annular source regions being laterally spaced along said first planar semiconductor surface from the facing respective edges of said common conduction region thereby to define first and second channel regions along said first planar semiconductor surface between each pair of said first and second annular source regions, respectively, and said common conduction region; each of said first and second channel regions being coplanar with one another;

a common source electrode means connected to said first and second annular source regions and their respective first and second base regions;

gate insulation layer means on said first planar semi-conductor surface, disposed at least on said first and second channel regions;

gate electrode means on said gate insulation layer means and overlying said first and second channel regions;

a drain conductive region remote from said common conduction region and separate therefrom by said relatively lightly doped major body portion and extending to said second semiconductor surface;

a drain electrode coupled to said drain conductive region; and

each of said at least first and second spaced base regions having [a polygonal configuration] *identical polygonal configurations*; each of said first and second annular source regions having a polygonal configuration conforming to that of their respective base region.

Please add new claims 15-20 as follows:

15. The device of claim 1 wherein said vertical common conduction region is disposed beneath said gate insulation layer means on said first surface.

16. The device of claim 3 wherein said vertical common conduction region is disposed beneath said gate insulation layer means on said first surface.

17. The device of claim 7 wherein said vertical common conduction region is disposed beneath said gate insulation layer means on said first surface.

18. The device of claim 8 wherein said vertical common conduction region is disposed beneath said gate insulation layer means on said first surface.

19. The device of claim 7 wherein said drain electrode is connected to said second semiconductor surface.

20. The device of claim 8 wherein said drain electrode is connected to said second semiconductor surface.

REMARKS

This is in response to the below-quoted rejections of the claims of U.S. Patent No. 5,008,725 (hereafter "the '725 patent"). For the reasons set forth below, reconsideration of the rejections is respectfully requested.

For the Examiner's convenience, the following is a Table of Contents of the points of argument made hereinafter:

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B. *"Claims 3, 5/3 and 13 are rejected under 35 U.S.C. 103 as being unpatentable over Takakuwa and Okabe et al. '878 as applied supra, but further considered with the Yoshida et al. IEEE article and the Lisiak et al. article"* Office Action, p. 6 21

C. *"Claims 1 and 5/1 are rejected under 35 U.S.C. 103 as being unpatentable over Takakuwa, Okabe et al. '878, Yoshida et al. IEEE and Lisiak et al. as applied supra, but further considered with Fukuta"* Office Action, p. 9 23

D. *"Claim 4 is rejected under 35 U.S.C. 103 as being unpatentable over Takakuwa, Okabe et al. '878, Yoshida et al. IEEE, Lisiak et al. and Fukuta, . . . but further considered with the Krishna article."* Office Action, p. 10 23

E. *"Claims 2, 6, 9 and 10 are rejected under 35 U.S.C. 103 as being unpatentable over Takakuwa, Okabe et al. '878, Yoshida et al. IEEE, Lisiak et al. and Fukuta as applied supra to Claims 1, 3, 7 and 8, but further considered with Lidow et al. '286, '666, '759 and '699 . . . ."* **Office Action, p. 11** 24

F. *"Claims 11 and 12 are rejected under 35 U.S.C. 103 as being unpatentable over Takakuwa, Okabe et al. '878, Yoshida et al. IEEE, Lisiak et al. and Fukuta, as accordingly applied supra to Claims 1, 3, 7 and 8, but further considered with Ishitani . . . corroborated by Lidow et al. '286, '666, '759 and '699, . . . Sakai '688 of record in Reexamination Control Number 90/002,478 (Reexam 2478), and presently provided Tihanyi et al., Plummer et al., Scharf et al. and Pocha et al., ..."* **Office Action, p. 12** 25

G. *"Claims 3, 5/3, 7, 8 and 14 are rejected under 35 U.S.C. 103 as being unpatentable over Hendrickson . . . , considered with presently cited and provided Lee and Declercq et al. . . . , but further considered with Ishitani . . . "* **Office Action, p. 14** 26

H. *"Claim 13 is rejected under 35 U.S.C. 103 as being unpatentable over Hendrickson, Lee, Declercq et al. and Ishitani, as applied supra, but further considered with the Lisiak et al. article."* **Office Action, p. 17** 28

I. *"Claim 4/3 is rejected under 35 U.S.C. 103 as being unpatentable over Hendrickson, Lee, Declercq et al. and Ishitani, as applied supra to Claim 3, but further considered with the Lisiak et al. article similarly as discussed supra with respect to Claim 13, but still further considered with the Krishna article . . . ."* **Office Action, p. 18** 28

J. *"Claims 6, 9 and 10 are rejected under 35 U.S.C. 103 as being unpatentable over Hendrickson, Lee, Declercq et al. and Ishitani as applied supra to Claims 3, 7 and 8, but further considered with Lidow et al. '286, '666, '759 and '699 . . ."* **Office Action, p. 18** 28

K. *"Claims 11/3, 11/7, 11/8, 12/11/3, 12/11/7 and 12/11/8 are rejected under 35 U.S.C. 103 as being unpatentable over Hendrickson, Lee, Declercq et al. and Ishitani as applied supra to Claims 3, 7 and 8, but again considered with Ishitani as corroborated by Lidow '286, '666, '759 and '666 . . . , Sakai '688, of record in Reexam 2478, and presently cited and provided Tihanyi et al., Plummer et al., Sharf et al. and Pocha et al. . . ."* **Office Action, p. 19** 29

L. *"Present Claims 7, 8 and 14 of US 5,008,725 (Claims 7, 8 and 14 '725) are rejected under the judicially established doctrine of obviousness-type double patenting as being unpatentable over Claim 1 of US 4,959,699 (Claim 1 '699) considered further with Takakuwa and Okabe et al."* **Office Action, p. 20** 29

M. *"Claims 3, 5/3 and 13 '725 are rejected under the judicially established doctrine of obviousness-type double patenting as being unpatentable over Claim 1 '699 considered with Takakuwa, Okabe et al., Yoshida et al. IEEE, and Lisiak et al."* **Office Action, p. 20** 30

N. *"Claims 1 and 5/1 '725 are rejected under the judicially established doctrine of obviousness-type double patenting as being unpatentable over Claim 1 '699 considered with Takakuwa, Okabe et al., Yoshida et al. IEEE, Lisiak et al. and Fukuta."* **Office Action, p. 21** 30

O. *"Claim 4 '725 is rejected under the judicially established doctrine of obviousness-type double patenting as being unpatentable over Claim 1 '699 considered with Takakuwa, Okabe et al. '878, Yoshida et al. IEEE, Lisiak et al., Fukuta and Krishna making obvious the claimed dimensions within a Takakuwa mesh-base MOSFET."* **Office Action, p. 21** 31

P. *"Claims 2, 6, 9 and 10 '725 are rejected under the judicially established doctrine of obviousness-type double patenting as being unpatentable over Claims 2 and 6 '699 considered with Takakuwa, Okabe et al. '878, Yoshida et al. IEEE, Lisiak et al. and Fukuta, as essentially discussed supra."* **Office Action, p. 22** 31

Q. *"Claims 11 and 12 '725 are rejected under the judicially established doctrine of obviousness-type double patenting as being unpatentable over Claim 7 '699 considered with Takakuwa, Okabe et al. '878, Yoshida et al. IEEE, Lisiak et al. and Fukuta, as essentially discussed supra."* **Office Action, p. 22** 31

VI. **SECONDARY CONSIDERATIONS COMPEL A CONCLUSION THAT CLAIMS 1-14 AND PROPOSED NEW CLAIMS 15-20 OF THE '725 PATENT ARE UNOBVIOUS FROM THE ART** 31

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VII. **CONCLUSION** 34

I. PROPOSED AMENDMENT TO CLAIMS 1, 3, 7 and 8

An amendment has been proposed for claims 7 and 8 to emphasize that the common conduction region between spaced bases is "vertical." Claims 1 and 3 have also been amended so that, like claims 7 and 8, they now emphasize that "the space between said polygonal base regions defin[es] a vertical common conduction region." As will be explained below, the prior art does not teach or suggest the '725 invention's use of a plurality of identical polygonal bases to define such a common conduction region.

II. PROPOSED NEW DEPENDENT CLAIMS 15-18

New dependent claims 15-18 are proposed to recite that the vertical common conduction region of independent claims 1, 3, 7 and 8, respectively, is disposed beneath the gate insulation layer means on the first surface. This additional element further emphasizes the differences between the '725 invention and certain of the prior art references.

III. PROPOSED NEW DEPENDENT CLAIMS 19-20

New dependent claims 19-20 are proposed to recite that, in addition to the vertical common conduction region of independent claims 7 and 8, the drain electrode is required to be on the surface opposite to that of the channel regions. This additional element further distinguishes the '725 invention from certain of the prior art references.

Accordingly, based upon the foregoing amendments and for the reasons set forth in detail below, patentee requests that the patentability of '725 claims 1-14 and new claims 15-20 be confirmed.

IV. THE STANDARD OF OBVIOUSNESS

The Examiner has combined fifteen (15) references in one of the rejections at issue and no less than fourteen (14) in another. Therefore, at the outset, the standard of obviousness should be stated.

The Federal Circuit has, in a dozen or more decisions, emphasized and required that the desirability of a combination of references in an obviousness determination must be supported in the references. A collection of such decisions will

be found in Roper Corp. v. Litton Sys. Inc., 757 F.2d 1266 (Fed. Cir. 1985). See also In re Bond, 910 F.2d 831, 834, 15 USPQ2d 1566 (Fed. Cir. 1990)("Obviousness cannot be established by combining the teachings of prior art to produce the claimed invention, absent some teaching, suggestion or incentive supporting the combination."). The Federal Circuit demands that both the suggestion and expectation of success be found in the prior art. In re O'Farrell, 853 F.2d 894, 903 (Fed. Cir. 1988).

The Examiner's rejections do not pass this test. As will be shown, the motivation or suggestion of the combinations cannot be found in the references, but comes only (if at all) from the hindsight knowledge of the claimed invention.

Accordingly, for the reasons discussed below, patentee submits that the rejection of claims 1-14 should be withdrawn.

V. THE REJECTIONS OF CLAIMS 1-14 ARE IN ERROR AND SHOULD BE WITHDRAWN.

A. *"Claims 7, 8 and 14 are rejected under 35 U.S.C 103 as being unpatentable over Takakuwa . . . , considered with Okabe et al. '878 . . . ."* Office Action, p. 2.

In this portion of the Office Action, the Examiner has taken a sentence fragment where the Takakuwa translation uses the word "mesh" and uses the Okabe reference to interpret what "mesh" must mean. It is respectfully submitted that this analysis is flawed, for several reasons. First, and most important, it is an analysis that is divorced from the rest of the Takakuwa reference -- both in the technical teachings of that reference and in its Japanese-language meaning. Second, for various technical reasons the Okabe reference does not provide any guidance or teachings on any subject of interest to a designer facing the challenges posed by Takakuwa.

Patentees believe that the McElroy translation of Takakuwa is serviceable, but requires careful reading and amplification in certain respects.[1] Attached hereto as

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[1] Requester has provided two translations -- the McElroy translation obtained by Requester and a second translation that Requester falsely suggests was (continued...)

Exhibit A is the Declaration of Toyu Yazaki in conjunction with this response which explains in greater detail the English-language ambiguities (created by Requester's arguments) that the McElroy translation contains that are not present in the Japanese-language original. As also explained in the Yazaki Declaration, the interpretation given Takakuwa by the Examiner (in light of Okabe) is directly contrary to the ideas communicated unambiguously by that reference in the Japanese language.

Takakuwa teaches a technique for avoiding breakdown in a vertical conduction MOSFET. Takakuwa does this by deliberately introducing a JFET structure into the MOSFET. Takakuwa describes his invention as increasing the "withstand voltage" of the device by reducing electric fields at the point where the thin gate oxide overlays the lightly doped drain region, which he labels "a." His concern is to avoid large voltages in the drain at point "a" that can cause breakdown at the gate oxide. This he accomplishes by using ring diffusion 17 to operate in conjunction with the base as a JFET to create a depletion layer. Takakuwa teaches that, by properly selecting the distance ℓ between the ring diffusion and the base, the JFET will "pinch off" the region between the ring and the base, and in that way allow the designer to reduce the voltage at the thin gate oxide, point *a*. Takakuwa's JFET-forming ring diffusion 17 does not contain a source and channel, because addition of these structures would produce an additional point *a* -- compounding the very weakness in Takakuwa's device he was trying to avoid.

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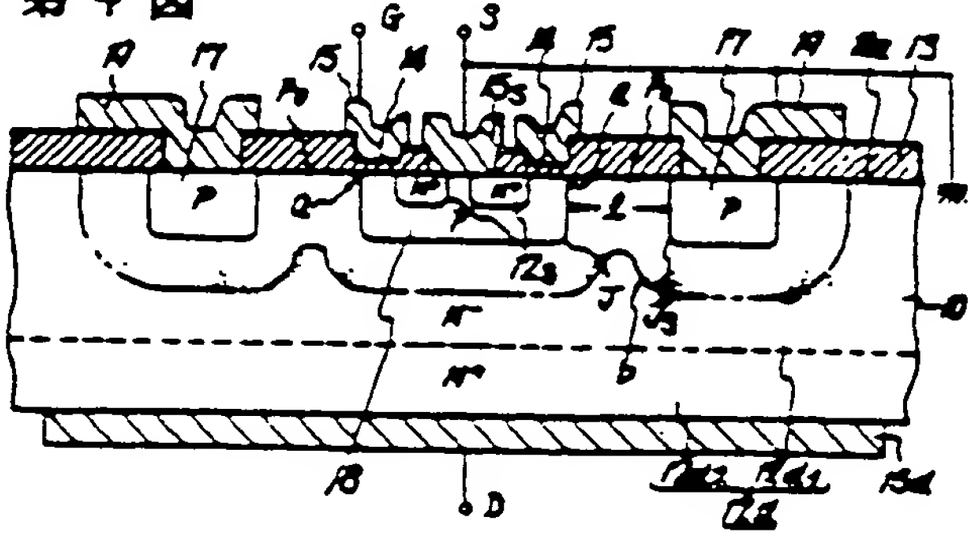
[1](...continued)
obtained by patentees (Request p. 14). In fact, that second translation was sent to patentee by NEC to support certain arguments NEC was making in connection with licensing discussions. It was produced to Requester in litigation pursuant to Requester's request for a copy of patentees' licensing files.

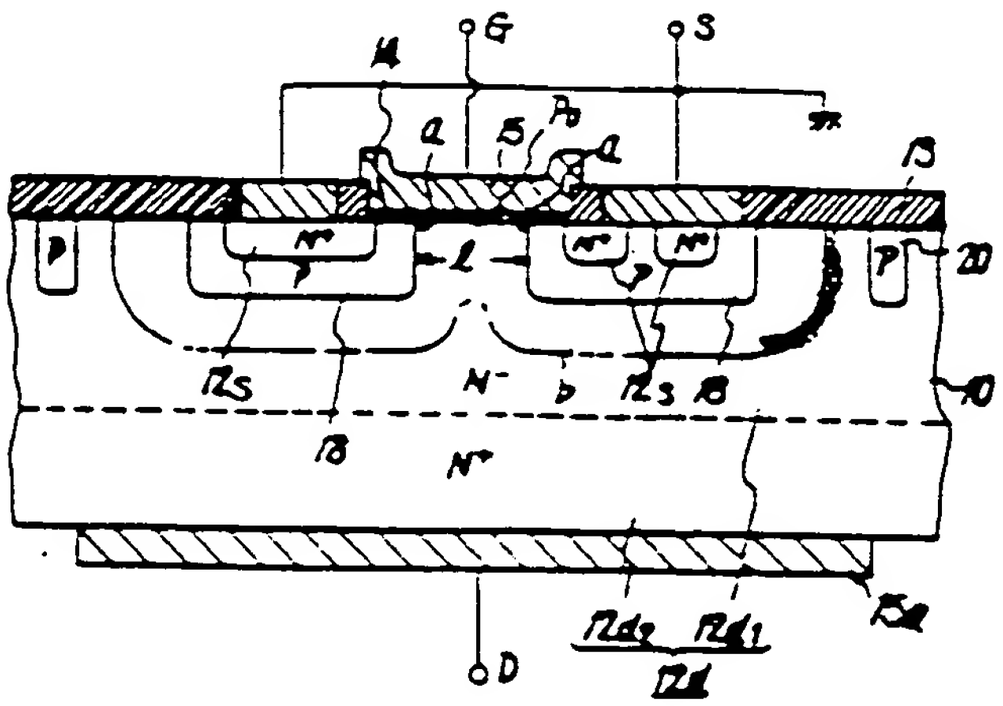
第４図



Ring diffusion spaced distance ℓ from base to form a JFET whose depletion layer will "pinch off" region *a* in Takakuwa Figure 3/4 device in off state.

After describing his basic invention (using a ring diffusion to form a JFET whose depletion layer "pinches off" the channel area) in terms of Figures 3 and 4, Takakuwa went on to describe an alternative version that did not require use of a specially formed ring. In this version, the base itself is formed into an annular ring, with a hole of width ℓ in the center. Thus, instead of the Figure 3/4 configuration of a square base with a channel on the *outer* perimeter of the base protected by a separate ring JFET, this structure (depicted in cross section in Figure 5 of the Takakuwa reference, which is reproduced below, again highlighting the depletion layer) employed an annular base with a channel on the *inner* surface of the annulus. As with the Figure 3/4 structure, the width ℓ is selected to "pinch off" the channel region *a* with the depletion layer formed by the base itself.

第 5 図



Ring-shaped base region with annular opening of width ℓ to form a depletion layer to "pinch off" region *a* in Takakuwa Figure 5 device in off state.

Thus, Takakuwa teaches (using the McElroy translation) that "it is not necessary to specially provide [ring] region 17." [p. 6.] Instead, Takakuwa teaches that "It is also possible, as shown in Figure 5, to form base region (18) and on top of it source region (12_s) each in a ring pattern . . . in such a way that spacing ℓ is maintained in a portion thereof and they oppose one another." In the next sentence, Takakuwa goes on to say that "It is also possible to form region (18) and region (12_s) . . . in such a way that . . . they form a mesh pattern, and the drain region (12_d) fits within the interstices of that mesh." [pp. 6-7.]

Takakuwa provides no top view of this further modified "mesh" structure. It is apparent from the text, however, that Takakuwa is suggesting that the annular base of Figure 5 could be modified to form multiple annular openings in a mesh-like pattern, with the drain fitting within the "interstices" of the mesh -- *i.e.*, the annular openings (or "holes" in the mesh) around which the channels are formed. Indeed, as explained by Mr. Yazaki, Takakuwa uses the Japanese term "ami mei nai" to describe the position of the drain region -- a term whose literal translation is "inside the eye of the net". This

Japanese term, even more than the McElroy use of the English term "interstices," is completely unambiguous concerning the relationship of the base and drain: Takakuwa teaches the formation of a single base either with a single annular opening permitting the drain to reach the top surface (as in Figure 5), or with multiple annular openings in a "mesh" or "net" pattern with the drain appearing in the "interstices" or "eyes" of that net. It is noteworthy in this regard that the prior art Ishitani patent[2] and Yoshida IEEE article[3] use the term "mesh" to describe similar single-base frame structures.

A simplified version of the Figure 5 structure and the "mesh" base structure are sketched on the following page (with the source regions shaded for clarity).

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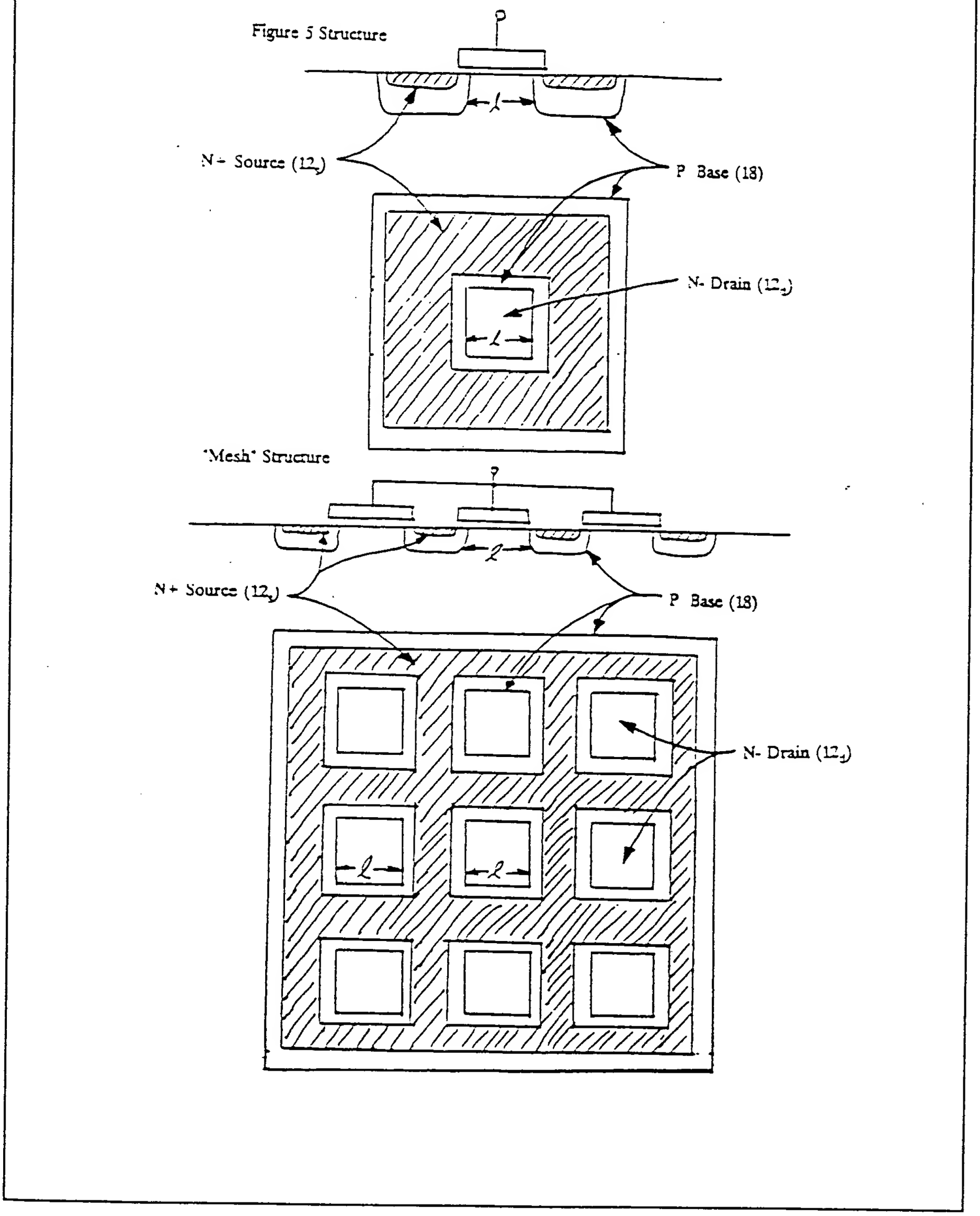
[2] Ishitani refers to the base as a "frame region" (col. 1, line 68 - col. 2, line 1) and further describes it as having a "comb-shape or mesh-shape" (col. 2, line 50).

[3] The title of the Yoshida article refers to a "meshed gate structure," which as is apparent from Figure 1(a) of the article describes a single gate electrode with square openings.



Takakuwa Figure 5 and "mesh" structures, simplified.

The central teaching of Takakuwa is that a JFET should be formed in order to protect the thin gate oxide from voltage stresses. Takakuwa teaches that there are two means of forming this JFET:

- A base region which has a conductive channel at the outer edge of the base should be surrounded by a separate p region (at the proper spacing ℓ and biased appropriately) in order to form a protective JFET. In this case, the drain-base junction is convex when viewed from the top surface.
- If the base is formed in the shape of an annulus so that the channel is on the inner surface, then there is no need for another p region for forming the JFET if the proper spacing ℓ is used for the annular opening. In this case, the drain-base junction is concave when viewed from the top surface.

Takakuwa also applies these teachings to describe three possible topologies:

- a square or rectangular base surrounded by a ring diffusion forming a JFET with spacing ℓ between the base and the ring,
- an annular base (or, equivalently, an elongated annulus forming a "belt" or "bands") with a channel on the inner annular surface of diameter ℓ, and
- a "mesh" structure where a single base forms a kind of "frame" around a series of lightly doped drain "eyes" or windows (of diameter ℓ).

None of these structures is even remotely described by the claims of the '725 patent, which at a minimum requires a number of spaced, polygonal bases defining a common conduction region. All of the Takakuwa structures have but a single base and no common conduction region.

While Takakuwa apparently realized the benefits of larger channel width for a given area of silicon in order to improve current handling capability, he limits his discussion of "meshed" devices (which will increase channel width) to structures with inner annular channels and a single base. Nowhere does Takakuwa suggest that it would be desirable to form a device out of an array of base regions.

Nor is Okabe of use, either in interpreting Takakuwa or in suggesting to those of skill that benefits could be derived by diverging from the Takakuwa teachings. Okabe's teaching concerns the use of spaced "gate" structures in a JFET to "pinch off" at **low** voltages -- indeed, Okabe strives to achieve pinch-off at as low a voltage as possible. Okabe contains no discussion at all concerning device performance at high voltages where breakdown would be a concern, which is of course the engineering problem addressed by Takakuwa.

Moreover, while Okabe plainly does <u>not</u> concern itself with a power MOSFET, it is also far from clear that Okabe depicts any relevant MOSFET structure. For example, although the structure depicted in cross section in Figure 2 of that reference (described in the reference only as a "field effect transistor") has an insulated gate electrode 13, that electrode is shown to be restricted to the <u>inner</u> surface of the "low concentration impurities" region 10. Even if one assumes that region 10 is a MOSFET base, the structure depicted in Figure 2 is most likely the cross section of a conventional <u>annular</u> base; moreover, it could <u>not</u> represent a cross section of a base array (which would necessarily have a gate electrode <u>surrounding</u> each base). In any event, there is nothing in Okabe that states or suggests that the "low concentration impurities" region 10 of Figure 2 could be analogized to one of the low-voltage JFET gate regions "2" depicted in cross section in Figure 1 and in top view in Figures 3 and 4.

B. ***"Claims 3, 5/3 and 13 are rejected under 35 U.S.C. 103 as being unpatentable over Takakuwa and Okabe et al. '878 as applied supra, but further considered with the Yoshida et al. IEEE article and the Lisiak et al. article"*** **Office Action, p. 6.**

For the reasons set forth above, Takakuwa, whether taken alone or in combination with Okabe, does not teach or suggest the use of spaced base regions in a power MOSFET. Yoshida IEEE and Lisiak also depict single-base structures and

provide no teachings or suggestions for the multiple-base configuration that is the essential prerequisite to any structure even remotely relevant to the '725 invention.

The Yoshida IEEE and Lisiak structures teach a method of improving lateral conduction MOSFET structures (devices where current flows along the top surface of the device, directly under the full width of the gate). As described in the Yoshida IEEE reference, these lateral-conduction structures did not handle large off-state voltages very well, were difficult to manufacture due to complicated electrode connections to the gate, source and drain on the top surface, and had at best modest channel width per unit area.

In the Yoshida IEEE and Lisiak designs, the junctions defining the MOSFET were based on lateral conduction designs with the current intended to flow laterally under the full width of the gate, but were improved by having the source and drain electrodes on opposite surfaces. While these structures were slightly less complicated to manufacture than lateral conduction structures (because two and not three connections had to be made on the top surface), in the words of Lisiak, these structures still had many design drawbacks:

> "The p+ drain electrode, although connected at the back, consumes surface area between the sources. This lateral design limits channel width packing density and could be a reliability problem, particularly at higher design voltages."

But for the extension of the central portion of each drain region to the underlying substrate, the Yoshida and Lisiak Figure 7(b) structures are the same as a lateral-conduction structure of alternating source and drain regions formed in a common base (this is why Lisiak refers to this structure as a "lateral design"). Thus, Yoshida/Lisiak has a single base frame defining an array of square openings that have the appearance of a "checkerboard" -- *i.e.*, there is an opening in the base frame only for every other square (like the black squares on a checkerboard). The alternate locations (like the red squares on a checkerboard) contain annular source diffusions. The insulated polysilicon gate electrode is contained within the lateral extent of the base frame between the annular sources and the openings in the base frame where the drain reaches the surface.

It is also noteworthy that Lisiak teaches that these drawbacks can be avoided by moving to a non-planar, V-groove design. He makes no suggestion that advantages could be gained by abandoning the single-base concept and moving to multiple bases directing current to flow vertically in a common conduction region, much less by replicating polygonal bases over the surface of a planar device.

As noted above, the characterization of the polysilicon gate in the Yoshida IEEE structure as "meshed" does not support the Examiner's interpretation of Takakuwa as suggesting multiple bases. To the contrary, both the gate and the base in the Yoshida IEEE structure is a single frame with square openings. If this "mesh" is used to interpret the Takakuwa "mesh," then again Takakuwa would be interpreted in a manner <u>opposite</u> to the interpretation advanced by the Examiner.

C. ***"Claims 1 and 5/1 are rejected under 35 U.S.C. 103 as being unpatentable over Takakuwa, Okabe et al. '878, Yoshida et al. IEEE and Lisiak et al. as applied supra, but further considered with Fukuta"*** **Office Action, p. 9.**

While the Examiner relies on Fukuta as teaching the desirability of using hexagonal drain regions, it is important to keep in mind that Fukuta discloses a lateral conduction device having a single base and openings distributed over the top surface for the drain and source regions. Although the embodiment cited by the Examiner uses hexagonal <u>drain</u> openings in this single base layer, Fukuta does not suggest that this lateral-conduction device could or should be modified to use hexagonal (or any other shape) spaced <u>bases</u> with current flowing vertically between those bases.

D. ***"Claim 4 is rejected under 35 U.S.C. 103 as being unpatentable over Takakuwa, Okabe et al. '878, Yoshida et al. IEEE, Lisiak et al. and Fukuta, . . . but further considered with the Krishna article."*** **Office Action, p. 10.**

As discussed above, all of the MOSFET references cited here employ a single base region or layer, with one (Takakuwa) employing vertical conduction and the remaining references employing lateral conduction (current flow in the on state parallel to the top surface under the width of the gate electrode). While Krishna describes the advantages of vertical over lateral conduction, he does not specify the topology that

should or could be employed. Indeed, the Krishna analysis makes no reference at all to junction curvature when viewed from above -- he calculates the depletion and space-charge layers without taking into account the effects of such junction curvature. In the context of Takakuwa, this provides at most further analytical support for the spacing ℓ between opposite sides of an annular opening (such as that depicted in Takakuwa Figure 5 or Krishna Figure 1b).

E. *"Claims 2, 6, 9 and 10 are rejected under 35 U.S.C. 103 as being unpatentable over Takakuwa, Okabe et al. '878, Yoshida et al. IEEE, Lisiak et al. and Fukuta as applied supra to Claims 1, 3, 7 and 8, but further considered with Lidow et al. '286, '666, '759 and '699 . . . ."* **Office Action, p. 11.**

Unlike the other references on which the Examiner relies, the Lidow references do depict the use of spaced bases -- in each case two separate, opposing base regions with a gate disposed between the bases so the two channel regions faced each other across a "common conduction region." One such structure used two elongated, closed base regions with no end points (like one bicycle tube laid inside a circle defined by slightly larger tube; these "tubes" are then scrunched to make a kind of serpentine or accordion pattern). Another structure used a square inner base within an annular square outer base. These bases minimized corner effects (which were felt to degrade breakdown performance by thinning the depletion layer at those corners in the off mode) -- there were no corners in the serpentine embodiment, and each corner in the square embodiment was opposed by a corner of the opposite curvature.

None of the references other than Takakuwa employs a vertical conduction structure, and so none is comparable to the Lidow references. As for Takakuwa, the square base embodiment of the Lidow references is an improvement over the Takakuwa Figure 3/4 structure in that the outer JFET ring has been replaced by a structure in which a channel could be formed opposing the channel formed in the inner square base. The Lidow references thus disclose structures containing a common conduction region between spaced bases, which is a fundamental improvement over Takakuwa.

There is nothing in those references, however, to suggest that a number of the inner square bases could be replicated so that they opposed one another rather than

being opposed by an annular region of the opposite curvature. This is a fundamental breakthrough of the '725 patent.

F. *"Claims 11 and 12 are rejected under 35 U.S.C. 103 as being unpatentable over Takakuwa, Okabe et al. '878, Yoshida et al. IEEE, Lisiak et al. and Fukuta, as accordingly applied supra to Claims 1, 3, 7 and 8, but further considered with Ishitani . . . corroborated by Lidow et al. '286, '666, '759 and '699, . . . Sakai '688 of record in Reexamination Control Number 90/002,478 (Reexam 2478), and presently provided Tihanyi et al., Plummer et al., Scharf et al. and Pocha et al., ..."* **Office Action, p. 12.**

Takakuwa is cumulative of Ishitani -- both disclose a vertical-conduction structure employing a base frame through which separate "islands" of drain region extend to the top surface. The channels in the Ishitani/Takakuwa structure take the form of an annulus, with current flowing inwardly through the channel into the central drain "island."

The Sakai '688 reference also discloses a vertical-conduction MOSFET structure -- a single annular base with conduction vertically through the central opening. This is confirmed by Sakai himself in his abandoned Japanese patent application Publication No. 53-135284, Nov. 25, 1978, translation p. 2.

Figure 5 of the Tihanyi reference also discloses a vertical conduction device, which is "symmetrical or rotation-symmetrical to a plane or axis of symmetry 20." No suggestion is made in Tihanyi that the base region is discontinuous. Tihanyi shows only an annular topology (e.g., the reference numerals on left and right in Fig. 5 are identical for the annular "deep base" 14, annular "shallow base" 13 and annular source 6, see 37 C.F.R. § 184(f)), and Tihanyi's text merely provides two alternative verbal descriptions of the illustrated annular (whether circular or elongated oval) geometry. The configuration, of course, is similar in layout to Takakuwa Figure 5 or the Takakuwa elongated "mutually opposed band patterns."

The Plummer, Scharf and Pocha references all depict lateral conduction devices with no relevance to the basic '725 invention of spaced, identical, polygonal bases defining a vertical common conduction region.

As above, the Lidow, Sakai, Tihanyi, Takakuwa and Ishitani references are the only ones to disclose vertical conduction structures, and of those only the Lidow

references employ spaced bases with a common conduction region. There is nothing in Lidow references (whether taken alone or in combination with the others) to suggest that the inner square base could be replicated so that a number of them opposed one another rather than having a single square base opposed by an annular region of the opposite curvature. This is a fundamental breakthrough of the '725 patent.

G. ***"Claims 3, 5/3, 7, 8 and 14 are rejected under 35 U.S.C. 103 as being unpatentable over Hendrickson . . . , considered with presently cited and provided Lee and Declercq et al. . . . , but further considered with Ishitani . . . "*** **Office Action, p. 14.**

Hendrickson teaches a number of strategies for increasing channel width per unit area for various field-effect transistor structures. After analyzing certain prior-art structures such as Fukuta and performing certain calculations, Hendrickson concludes that arrays of triangular regions provide the greatest possibility for channel width per unit area. (col. 8, lines 22-26, col. 9, lines 61-64.) Hendrickson then describes field-effect transistor structures implemented according to the preferred triangular layout.

Hendrickson first describes his invention in terms of JFETs and in connection with lateral-conduction MOSFETs. These structures are depicted in top view in Figures 6, 7, 10 and 11 and in cross-section in Figures 8, 9 and 12. The MOSFET of Figure 8 has a single base region into which alternating triangular source and drain regions have been diffused, while the MOSFET of Figure 12 has spaced triangular bases, each having a solid triangular source. Both of those MOSFET structures are lateral-conduction because the current flows from source to drain under the width of the gate along the top surface of the device.

The planar MOSFETs of Hendrickson Figures 8 and 12 are wholly unlike the MOSFETs described and claimed in the '725 patent. Most fundamentally, Hendrickson describes lateral conduction planar MOSFETs, not vertical conduction MOSFETs of the kind described and claimed in the '725 patent. Moreover, there is no indication that Hendrickson even considered the breakdown voltage performance of his planar MOSFET structures. Due to their unprotected sharp corners, they would not be suitable for high voltage operation, and would likely break down with only a few tens of volts applied between source and drain in the off condition. The Hendrickson structures

would also require that the top electrode layer be interdigitated between source and drain electrodes.

Hendrickson also purports to apply the geometrical analysis of planar, lateral conduction MOSFETs and JFETs to V-groove structures, both vertical and lateral conduction. Because, however, grooved structures at that time could effectively be made only with right angles at the surface, it would be impractical to construct Hendrickson's grooves with a triangular surface expression, as the Examiner has recognized.

Even assuming Hendrickson's vertical conduction V-groove structures were valid practical structures, or could be modified in accordance with the teachings of Lee and Declercq to employ right-angle geometries, they would still be fundamentally different from the planar structures employed in the '725 patent. First, one of the principal objects of the '725 patent was to avoid the inherent drawbacks of grooved structures by employing planar structures having fundamentally different design considerations. Moreover, the Hendrickson V-groove structure does not employ spaced bases, but rather has a single sheet P type region disposed atop an N type drain region, with the P region penetrated by grooves defining the channels.

While Ishitani recognized and sought to avoid these and other drawbacks inherent in V-groove structures (col. 1, lines 52-56), there is no suggestion in Ishitani or anywhere else that describes how to transform a V-groove geometry such as Hendrickson's into any kind of planar structure (much less a spaced-base structure) or even whether it was possible to do so. For example, if we assume Hendrickson taught those of skill that it was desirable to construct bottom-drain devices with V-grooves having a square surface expression, with those grooves penetrating a buried "base" layer, and we further assume that Ishitani taught the desirability of using a vertical-conduction, planar base frame, the most that could be said would be that those of skill would understand the desirability of square channel regions (the downwardly conducting square channels of Hendrickson, and the inwardly conducting square channels of Ishitani). But there is no teaching in Ishitani or anywhere else that the actual planar topology disclosed in Ishitani could or should be reversed to form <u>spaced</u> bases (instead of Ishitani's single "frame" or "mesh-shape" base) with <u>outwardly</u> conducting square channels (instead of

Ishitani's inwardly conducting channels) and with a continuous drain region at the surface (instead of Ishitani's drain "islands" at the top surface).

H. ***"Claim 13 is rejected under 35 U.S.C. 103 as being unpatentable over Hendrickson, Lee, Declercq et al. and Ishitani, as applied supra, but further considered with the Lisiak et al. article."*** **Office Action, p. 17.**

As above, none of these references has anything to do with spaced-base, planar, vertical-conduction structures such as those claimed in the '725 patent.

The Lisiak article sought to avoid the drawbacks of the Yoshida IEEE planar "extended drain" structure by taking the Hendrickson approach to its logical conclusion: a "two-dimensional grid" of grooves penetrating a single base layer (p. 779). As Ishitani, observed, however, this design also had serious drawbacks, which Ishitani sought to cure with a vertical-conduction, planar, single-base design. None of these references suggest replicating separate, planar, polygonal bases as in the '725 invention.

I. ***"Claim 4/3 is rejected under 35 U.S.C. 103 as being unpatentable over Hendrickson, Lee, Declercq et al. and Ishitani, as applied supra to Claim 3, but further considered with the Lisiak et al. article similarly as discussed supra with respect to Claim 13, but still further considered with the Krishna article . . . ."*** **Office Action, p. 18.**

As above, none of these references has anything to do with spaced-base, planar, vertical-conduction structures such as those claimed in the '725 patent.

J. ***"Claims 6, 9 and 10 are rejected under 35 U.S.C. 103 as being unpatentable over Hendrickson, Lee, Declercq et al. and Ishitani as applied supra to Claims 3, 7 and 8, but further considered with Lidow et al. '286, '666, '759 and '699 . . ."*** **Office Action, p. 18.**

As above, none of these references, except the Lidow references, has anything to do with spaced-base, planar, vertical-conduction structures such as those claimed in the '725 patent. There is nothing in any of those references to suggest that a number of the inner square bases could be replicated so that they opposed one another rather than being opposed by an annular region of the opposite curvature. This is a fundamental breakthrough of the '725 patent.

K. *"Claims 11/3, 11/7, 11/8, 12/11/3, 12/11/7 and 12/11/8 are rejected under 35 U.S.C. 103 as being unpatentable over Hendrickson, Lee, Declercq et al. and Ishitani as applied supra to Claims 3, 7 and 8, but again considered with Ishitani as corroborated by Lidow '286, '666, '759 and '666 . . . , Sakai '688, of record in Reexam 2478, and presently cited and provided Tihanyi et al., Plummer et al., Sharf et al. and Pocha et al. . . ."* **Office Action, p. 19.**

As above, none of these references, except the Lidow references, has anything to do with spaced-base, planar, vertical-conduction structures such as those claimed in the '725 patent. There is nothing in any of those references to suggest that a number of the inner square bases could be replicated so that they opposed one another rather than being opposed by an annular region of the opposite curvature. This is a fundamental breakthrough of the '725 patent.

L. *"Present Claims 7, 8 and 14 of US 5,008,725 (Claims 7, 8 and 14 '725) are rejected under the judicially established doctrine of obviousness-type double patenting as being unpatentable over Claim 1 of US 4,959,699 (Claim 1 '699) considered further with Takakuwa and Okabe et al."* **Office Action, p. 20.**

The claims of the '699 and '725 patent differ most significantly in that claims of the '725 patent call for "a plurality of symmetrically disposed laterally distributed identical polygonal base regions" which receive respective annular source regions. Neither the claims of the '699 patent nor any of the cited secondary references disclose, suggest or make obvious either individually or in any combination, this key limitation of the claims of the '725 patent.

The '699 patent claims clearly do not recite identical polygonal base regions. Instead, Lidow and Herman, in their earlier work which ultimately led to the invention of the '725 patent, conceived of a polygonal cell which is opposed by a base of the opposite curvature ('699 Figs. 7 and 8). While the '699 patent claims, reciting a polygonal cell used in connection with a vertical common conduction region, describe and cover the individual cells in modern MOSFETs (a polygonal base surrounded by a common conduction region), they do not render obvious or even remotely suggest the replication of such a cell over the surface of a chip as recited in the claims of the '725 patent. This latter invention required the elimination of the annular outer base disclosed

in the '699 specification (*i.e.*, the base supplying the opposing corners having curvatures opposite to those of the polygonal base).

As previously stated, Takakuwa discloses a single base frame and does not suggest the claimed subject matter of the '725 patent. The square base embodiment of the '699 patent is an improvement over the Takakuwa Figure 3/4 structure in that the outer JFET ring has been replaced by a structure in which a channel could be formed opposing the channel formed in the inner square base. The '699 patent thus discloses structures containing a common conduction region between spaced bases, which is a fundamental improvement over Takakuwa.

There is nothing in those references, however, to suggest that a number of the inner square bases could be replicated so that they opposed one another rather than being opposed by an annular region of the opposite curvature. This is a fundamental breakthrough of the '725 patent.

M. ***"Claims 3, 5/3 and 13 '725 are rejected under the judicially established doctrine of obviousness-type double patenting as being unpatentable over Claim 1 '699 considered with Takakuwa, Okabe et al., Yoshida et al. IEEE, and Lisiak et al."*** **Office Action, p. 20.**

For the same reasons as set forth above, neither the '699 specification nor its claims suggest the replication of identical polygonal cells (although the claims of the '699 patent cover such an individual cell). Nor do any of the other cited references suggest such structures.

N. ***"Claims 1 and 5/1 '725 are rejected under the judicially established doctrine of obviousness-type double patenting as being unpatentable over Claim 1 '699 considered with Takakuwa, Okabe et al., Yoshida et al. IEEE, Lisiak et al. and Fukuta."*** **Office Action, p. 21.**

For the same reasons as set forth above, neither the '699 specification nor its claims suggest the replication of identical polygonal cells. Nor do any of the other cited references suggest such structures.

O. *"Claim 4 '725 is rejected under the judicially established doctrine of obviousness-type double patenting as being unpatentable over Claim 1 '699 considered with Takakuwa, Okabe et al. '878, Yoshida et al. IEEE, Lisiak et al., Fukuta and Krishna making obvious the claimed dimensions within a Takakuwa mesh-base MOSFET."* **Office Action, p. 21.**

For the same reasons as set forth above, neither the '699 specification nor its claims suggest the replication of identical polygonal cells. Nor do any of the other cited references suggest such structures.

P. *"Claims 2, 6, 9 and 10 '725 are rejected under the judicially established doctrine of obviousness-type double patenting as being unpatentable over Claims 2 and 6 '699 considered with Takakuwa, Okabe et al. '878, Yoshida et al. IEEE, Lisiak et al. and Fukuta, as essentially discussed supra."* **Office Action, p. 22.**

For the same reasons as set forth above, neither the '699 specification nor its claims suggest the replication of identical polygonal cells. Nor do any of the other cited references suggest such structures.

Q. *"Claims 11 and 12 '725 are rejected under the judicially established doctrine of obviousness-type double patenting as being unpatentable over Claim 7 '699 considered with Takakuwa, Okabe et al. '878, Yoshida et al. IEEE, Lisiak et al. and Fukuta, as essentially discussed supra."* **Office Action, p. 22.**

For the same reasons as set forth above, neither the '699 specification nor its claims suggest the replication of identical polygonal cells. Nor do any of the other cited references suggest such structures.

VI. SECONDARY CONSIDERATIONS COMPEL A CONCLUSION THAT CLAIMS 1-14 AND PROPOSED NEW CLAIMS 15-20 OF THE '725 PATENT ARE UNOBVIOUS FROM THE ART

"Objective evidence of nonobviousness must always when present be considered en route to a determination [of the question] of obviousness because: 'evidence of secondary considerations may often be the most probative and cogent evidence in the record. It may often establish that an invention appearing to have been obvious in light of the prior art was not. It is to be considered as part of all the

evidence, not just when the decision maker remains in doubt after reviewing the art.'", Uniroyal Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 1053 (Fed. Cir. 1988), cert. denied, 488 U.S. (1988).

In the present case, a number of secondary considerations are present.

A. THE INVENTION OF THE '725 PATENT ENJOYED IMMEDIATE AND LASTING COMMERCIAL SUCCESS.

In 1979, the plural identical base configuration for power MOSFETs was introduced by International Rectifier, the assignee of the '725 patent. (Lidow ¶ 4.) Near-universal use of the '725 invention continues to this day -- it is still the basis of International Rectifier's power MOSFET line and is the geometry of choice of all modern MOSFET manufacturers in view of its inherent high packing density and large channel width and resulting low on-resistance for a given area of silicon. (Lidow ¶ 5.)

The following chart summarizes IR's total sales of Power MOSFETs employing the invention of the '725 patent beginning in 1979:

Year	Sales Using the '725 Invention
1979 (3rd & 4th quarter)	$ 868,000
1980	$ 4,459,000
1981	$ 8,530,000
1982	$ 13,192,000
1983	$ 25,558,000
1984	$ 38,492,000
1985	$ 51,480,000
1986	$ 44,978,000
1987	$ 56,724,000
1988	$ 89,961,000
1989	$100,333,000
1990	$132,709,000

1991	$147,136,000
1992	$163,202,000
1993	$177,643,000
1994	$216,531,000

(Lidow ¶ 6.)

Cumulatively, IR's sales, the sales of its licensees (discussed below) and the sales of its products by others under private label account for about 50% to 60% of the world's Power MOSFET sales. IR has since 1978 been, and continues to be, the acknowledged technology leader in Power MOSFETS. (Lidow ¶ 11). The invention of the '725 patent has experienced unquestionable commercial success.

The commercial success of the '725 patent is another secondary consideration which proves the nonobviousness of the invention.

B. THE '725 PATENT HAS BEEN WIDELY RESPECTED BY THE POWER MOSFET INDUSTRY

Another indicator of non-obviousness of an invention is respect of the invention by the industry. In the present case, as stated in the attached Declaration of Alexander Lidow, the '725 patent is the subject of post-issuance royalty-bearing licenses between International Rectifier and the following major power MOSFET manufacturers: NEC, Harris Corporation and Mitsubishi. Lidow ¶¶ 8-10. The recognition of the '725 patent by these respected international corporations is further significant evidence of the non-obviousness of the invention set forth in the '725 patent.

C. THE SECONDARY CONSIDERATIONS RELATING TO THE SUCCESS OF THE '725 INVENTION ARE OVERWHELMING

The Federal Circuit precedent cited above mandates that the Examiner consider secondary considerations in evaluating the patentability of the '725 invention. Patentee submits that the foregoing secondary considerations overwhelmingly establish the non-obviousness of the '725 invention.

VII. CONCLUSION

For all the above reasons, it is requested that the Examiner confirm the patentability of all the claims of U.S. Patent 5,008,725.

Respectfully submitted,

Stephen A. Soffen
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OSTROLENK, FABER, GERB & SOFFEN
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Telephone: (202) 457-7785

CERTIFICATE OF SERVICE

The undersigned hereby certifies that a true and correct copy of the foregoing "AMENDMENT PURSUANT TO 37 C.F.R. § 1.550(b)" is being served on the attorneys for Requester SGS-Thomson Microelectronics, Inc. by sending a true copy of such document by first class mail, postage prepaid, on March 24, 1995 to the address set forth below.

Lisa K. Jorgenson
Patent Counsel
SGS-Thomson Microelectronics, Inc.
1310 Electronics Drive
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Stephen A. Soffen

Exhibit A

DECLARATION OF TOYU YAZAKI

I, Toyu Yazaki, declare as follows:

1. I am a native speaker of Japanese. I moved from Japan to the United States when I was 18 to attend college in the United States. Since 1980, I have worked full time as a free-lance translator and interpreter. I have been accredited by the United States Department of State as a "Conference Level" Japanese interpreter, which is the highest level possible. I frequently act as a translator and interpreter for high level governmental delegations, such as Prime Minister Nakasone's visit to San Francisco in 1988. A copy of my professional resume is attached hereto as Exhibit A.

2. I have read the Japanese-language patent document 51-134076, which I understand is referred to as the "Takakuwa" reference. I have also read the English-language translation of that document, which I understand was obtained by SGS-Thomson Microelectronics ("ST") and has been referred to as the "McElroy" translation. I have become acquainted with ST's argument that the McElroy translation suggests that Takakuwa describes a MOSFET structure with multiple square bases, each of which is surrounded by a continuous drain region. For the reasons set forth below, ST's arguments concerning the McElroy translation of Takakuwa are completely unsupported by the Japanese-language Takakuwa reference.

3. I have focused my attention on the complete paragraph in the upper left-hand quadrant of page 403 of the Japanese-language Takakuwa reference, and have compared my reading of that Japanese reference with the corresponding portion of the McElroy translation spanning pages 6 and 7. In the original Japanese, Takakuwa states that the base region 18 can be formed in a mesh pattern, with the drain region appearing in the "ami mei nai" -- which is a Japanese term that literally translates as "inside the eyes of the net." This term is used in Japanese to refer to openings in a mesh or similar structure -- for example, the opening in a screen or colander are the "ami mei" (the "net eyes"). In my opinion, this Japanese terminology, especially when viewed in conjunction with the figures and remaining text of the Takakuwa reference, precludes the interpretation advanced by ST. In my opinion, Takakuwa discloses not multiple base regions 18 each surrounded by a single, continuous drain, but rather describes a single base region 18 that contains a number of openings ("ami mei") through which the drain can be seen from the top surface.

I declare under penalty of perjury that the foregoing is true and correct.

Executed March 23, 1995 at San Francisco, California.

Toyu Yazaki

Exhibit A

Resume
of
Toyu Yazaki

Address: 391 Sutter St., Ste. 601, San Francisco, CA 94108
Phone: (415) 391-9308 FAX: (415) 391-9310

Personal Data

Place of birth: Tokyo, Japan

Educational Background

1972-1973: North Seattle Community College
1973-1975: Claremont Men's College, Claremont, CA
Major: Economics/Management Engineering
1982-1984: Stanford University, Stanford, CA
Major: Industrial Engineering

Work Experience

1980-1982: Tokyo Broadcasting System (TBS), Tokyo, Japan
Translation of nightly network news for broadcast in Japan. (TBS is the largest commercial television network in Japan.)
1984-present: Freelance translation and interpretation

Litigation Interpretation

IBM v. Hitachi (interpreter for Hitachi defense team)
Reference: Geoffrey Channon, Esq., John Keker, Esq., *Keker & Brockett*, San Francisco, CA

Intel v. NEC (court interpretation and interpreter for Intel)
Reference: Lois Abraham, Esq., Dan Kumamoto, Esq., *Brown & Bain*; Palo Alto, CA

Kikusui Electronics v. Tektronix (deposition interpretation)
Reference: Dennis Wong, Esq., *Cartwright, Slobodin*; San Francisco, CA; Peter Peckarsky, Esq., *Majestic, Parsons, Siebert & Hsue*, San Francisco CA

United States International Trade Commission investigation (Interpreter for Toho Titanium Co., Ltd.)
Reference: Robert Taylor, Esq., *Pillsbury, Madison & Sutro*, San Francisco, CA

SGS Thomson v. Seiko Epson (consultation for interrogation of Japanese witnesses, 1991)
Reference: David Carlson, Esq., *Seed and Berry*, Seattle, WA

Honda Motor Co. v. Mullins (trial interpretation, 1990)
Reference: Vincent Walkowiak, Esq., *Fulbright & Jaworski;* Dallas, Texas

Honda Motor Co. v. Jones (trial interpretation, 1992)
Reference: Dennis Seley, Esq., *Mackenroth, Seley & Arwyl*, Sacramento, CA

Honda Motor Co. v. David Moore (trial interpretation, 1993)
Reference: Robert Lynch, Esq., *Lynch, Loofbourrow, Helmenstine, Gilardi & Grummer*, San Francisco, CA

Honda Motor Co. v. Grace Feurtado (trial interpretation, 1993)
Reference: Anthony Sonnet, Esq., *Lester, Schwab, Katz & Dwire*, Torrance, CA

Honda Motor Co. v. Royston (trial interpretation, June 1993)
Reference: Larry Duplass, Esq., *Duplass, Witman, Zwain & Williams*, New Orleans, LA

Honda Motor Co. v. Utt (trial interpretation, January 1995)
Reference: Evan A. Douthit, Ewq., *Baker Sterchi & Cowden*, Kansas City, MO

Extensive experience in deposition and trial interpretation for product liability and patent infringement cases involving Japanese corporate defendants and plaintiffs.

Expert Witness

International Rectifier Corporation v. Siliconix Inc. (trial testimony as expert witness)
Reference: William Bohler, Esq., *Townsend & Townsend*; Palo Alto, CA

International Rectifier Corporation v. S.G. S. Thompson
Reference: Glenn W. Trost, Esq., *O'Melveny & Myers*, Los Angeles, CA

Non-litigation interpretation

U.S. State Department conference-grade certified simultaneous interpreter ("conference grade" is the highest certification grade granted by the U.S. State Department)

Canadian State Department conference-grade certified simultaneous interpreter

Simultaneous interpreter for annual International Labor Organization plenary sessions held in Geneva, Switzerland every June

Interpreter for former Japanese Prime Minister Yasuhiro Nakasone during San Francisco visit, April 1988

Interpreter, G7 Jobs Summit, Detroit, MI, Feb. 14-15, 1994, attended by President Clinton, Vice President Gore, Secretary of Labor Reich, Secretary of Commerce Brown, et al.

Interpreter, Asia-Pacific Leaders' Roundtable, Jan. 14 - 18, 1995; participated by U.S. Senator Bill Bradley, fomer Japanese Foreign Minister Ichiro Ozawa, former U.S. Secretary of State George P. Schultz, and former and present foreign ministers of Australia, Republic of Korea, Republic of China, Thailand and Singapore.

Translation

Specializing in the translation of *Japanese patents* and *technical literature for litigation discovery purposes.*

List of translated books

Title: 1985 Nippon Handohtai Nenkan ("*1985 Japan Semiconductor Annual*")
Publisher: All Press Journal

Title: Fuji Shashin Firumu Tai Konishiroku Shashin Kogyo ("*Fuji Photo Film Vs Konishiroku Photo Industry*")
Publisher: Hyogensha
Author: Shigeyuki Niitsu

Title: NPS No Kiseki ("*The Miracles Being Wrought by the New Production System*")
Author: Isao Shinohara
Publisher: Toyo Keizai Shinposha

Title: Kaizen Teian Handobukku ("*Improvement Suggestion Handbook*")
Publisher: Kindai Keieisha

IR 2.064 (2-838)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Patent Of:	
ALEXANDER LIDOW et al.	
Patent No. 5,008,725	DECLARATION OF ALEXANDER LIDOW
Reexamination Control No: 90/003,495	
Filing Date: July 15, 1994	
Examiner: James J. Carroll	
Group Art Unit: 2508	

I, Alexander Lidow, hereby declare and state:

1. I am a co-inventor with Thomas Herman and Vladimir Rumennik of U.S. Patent 5,008,725 ("the '725 patent").

2. I am Chief Executive Officer of the International Rectifier Corporation ("IR").

3. Messrs. Herman, Rumennik and I made the invention claimed in the '725 patent.

4. In 1979, IR introduced its first cellular high voltage MOSFETs employing the invention of the '725 patent.

5. The devices using the '725 invention were an immediate commercial success. IR's line of power MOSFETs was so popular that IR could not keep up with demand until after about 1983. IR still uses the patented concept of the '725 patent in its Power MOSFETs, IGBTs and power integrated circuits.

I declare under penalty of perjury that the foregoing is true and correct.

Executed this 23rd day of March 1995 at El Segundo, California.

Alexander Lidow